PATENT ABSTRACTS OF JAPAN

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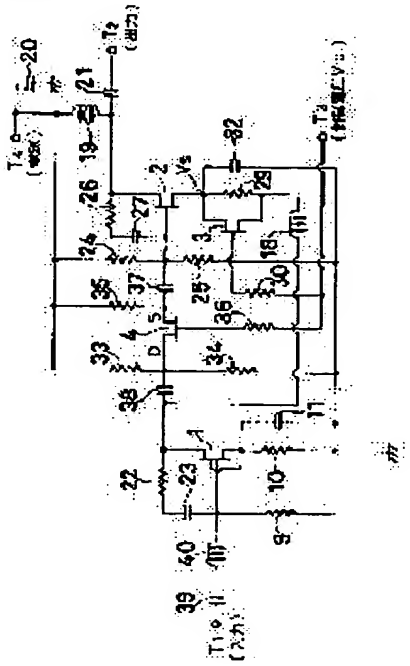
(54) HIGH FREQUENCY GAIN VARIABLE AMPLIFIER CIRCUIT

(57)Abstract:
PROBLEM TO BE SOLVED: To have a circuit operate with low current consumption, to reduce the deterioration of input/output reflection characteristic when the gain is variable and to secure stable operation, even in the case of expanding a variable gain width.
SOLUTION: A first FET 1 on the side of an input terminal T1 and a second FET 2 on the side of an output terminal T2 are connected to serially share the power source current of a power source terminal T3, when a ground potential is viewed from the terminal T3, and to operate by a low current. In addition, a third FET 3 and a resistor 29 provided with a variable resisting function are arranged between the first and second FETs 1 and 2, and a capacitor 32 for grounding by a high frequency is connected between the source/ground potential of this second FET 2. Thus, the deterioration of output reflecting characteristic at gain variation is suppressed. In addition, a fourth FET 4 with the function of a signal attenuator is together provided with bias resistors 33 to 35, to improve the linearity of the inclination of total gain variable characteristic.



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* NOTICES *

CLAIMS

[Claim(s)]
[Claim 1] The 1st transistor which inputs a RF signal into a gate electrode, and the 2nd transistor which outputs the RF signal concerned from a drain electrode, An inductor element or a resistance element for connecting between a drain electrode of the 1st transistor of the above, and a source electrode of the 2nd transistor of the above, and enlarging the above-mentioned inter-electrode RF-isolation, A capacitative element which makes low a RF-impedance in a source electrode of the 2nd transistor of the above, An implication and the 1st and 2nd transistors of the above consider as a configuration which shares current from a power supply to a serial. As a variable resistive element to which gain acquired with the 1st and 2nd transistors of the above, without changing a RF-output impedance of the 2nd transistor of the above is changed A RF gain adjustable amplifying circuit characterized by connecting to a serial a resistance element arranged to the 3rd transistor and the drain source inter-electrode of this 3rd transistor to the above-mentioned inductor element or a resistance element between the above 1st and the 2nd transistor.
[Claim 2] It connects between a drain electrode of the 1st transistor of the above, and a gate electrode of the 2nd transistor of the above. Gain adjustable control voltage impressed to a gate electrode of the 3rd transistor of the above which carries out adjustable [of the gain which prepares the 4th transistor which operates as a signal attenuator, and is acquired from the 1st and 2nd transistors of the above] It connects also with a gate electrode of the 4th transistor of the above. Between a drain electrode of the 4th transistor of the above, and the above-mentioned power supplies, Between a drain electrode of this 4th transistor, a source electrode of between touch-down potentials and the 4th transistor of the above, the above-mentioned power supply, or touch-down potential Gain variable characteristics with the 3rd transistor of the above A RF gain adjustable amplifying circuit of the claim 1 above-mentioned publication characterized by connecting a bias resistance element for amending the linearity of dip of comprehensive gain variable characteristics over gain adjustable control voltage of a signal damping property with the 4th considered transistor of the above.
[Claim 3] The above-mentioned bias resistance element arranged to a source electrode side of the 4th transistor of the above is above-mentioned claim 1 characterized by constituting so that it may serve also as bias resistance of a gate electrode of the 2nd transistor of the above, or a RF gain adjustable amplifying circuit given in two.
[Claim 4] A resistance element and a capacitative element are connected to a serial each drain gate inter-electrode of the 1st transistor of the above, and the 2nd transistor. The 1st transistor of the above and the 2nd transistor are constituted as wideband amplifier. Between the above-mentioned input terminal and a gate electrode of the 1st transistor of the above Above-mentioned claim 1 characterized by connecting an inductor element for seeing from this input terminal and amending an input reflection property in specific frequency thru/or a RF gain adjustable amplifying circuit given in three.
[Claim 5] Above-mentioned claim 1 characterized by forming a gain adjustable amplifying circuit of the above-mentioned configuration as an integrated circuit thru/or a RF gain adjustable amplifying circuit given in four.

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* NOTICES *

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[The technical field to which invention belongs] This invention relates to the configuration of an amplifying circuit with the gain adjustable function for signals, such as semi- microwave, from a RF gain adjustable amplifying circuit, especially an ultrashort wave.
[0002]
[Description of the Prior Art] From the former, the amplifying circuit which carries out adjustable control of the gain of a RF signal in the communication device handling signals, such as semi- microwave, etc. is used from the ultrashort wave, and there are some which are shown, for example in drawing 8 as this kind of an amplifying circuit from it. In drawing 8 , to the input terminal T1 which impresses a RF signal To the output terminal T2 which outputs the RF signal which the 1st field-effect transistor (it considers as Following FET) 1 of dual gate structure was connected through the input matching circuit 6, and performed amplification processing In order to make it not make deterioration of the output reflection property of the 1st above FET 1 influence the latter part at the time of gain adjustable, 2nd FET2 is connected through the input matching circuit 7.
[0003] In order to secure that actuation to the 1st above FET 1, resistance 12 and 13 and capacity 14 are arranged in the location of a graphic display at resistance elements (it considers as resistance below) 9 and 10 and a capacitative element (it considers as capacity below) 11, and FET2 of another side, and these capacity 11 and 14 carries out the duty which grounds the source electrode (it considers as the source below) of each FET 1 and 2 in RF. Moreover, between the 1st FET1 drain (it considers as a drain below), and the gate electrode (it considers as the gate below) of 2nd FET2, capacity 15 is connected for DC cut and impedance matching.
[0004] And terminal T3 for giving gain control voltage to the 2nd gate of 1st FET1 of the above-mentioned dual structure through resistance 16 It is arranged and the gain of the signal outputted from 2nd FET2 based on this gain control voltage is controlled. Moreover, inductors 18 and 19 are arranged between the drain of these 1st FET1 and 2nd FET2, and power supply terminal T four, and the RF-isolation between the drains of each FET 1 and 2 becomes high by these inductors 18 and 19. In addition, the above-mentioned power supply terminal T four is grounded in RF through capacity 20.
[0005] According to the gain adjustable amplifying circuit of such a configuration, stable actuation in a predetermined gain range is realizable in the form where deterioration of the output reflection property of 1st FET1 is not made to influence the latter part by 2nd FET2. That is, when not using the 2nd above FET 2, and gain control voltage is impressed to the 2nd gate electrode of the 1st above FET 1 and gain is changed to it, since change of the output reflection property of 1st FET1 is large, the filter and amplifier linked to the latter part of 1st FET1 will be affected, and aggravation and unstable actuation of a communication unit system etc. of a property will be caused.
[0006]
[Problem(s) to be Solved by the Invention] However, in a conventional circuit like above-mentioned drawing 8 , the new current for operating the 2nd added above FET 2 was needed,

and there was a problem that low consumed-electric-current actuation was unrealizable.
[0007] Moreover, when changing amplification gain, and deterioration of an output reflection property cannot fully be suppressed but it is moreover made to operate in a broadband even when the 2nd above FET 2 has been arranged, there is also nonconformity that deterioration of an input reflection property arises on specific frequency. Furthermore, when adjustable width of face of the above-mentioned gain is made into the circuitry made large, there is also a problem of being hard coming to secure the stable actuation in consideration of the linearity of the dip of comprehensive gain variable characteristics etc.
[0008] It is in offering the RF gain adjustable amplifying-circuit structure where the actuation stabilized even when deterioration of an I/O reflection property became small and adjustable gain width of face was made large, even if this invention is made in view of **** between the above, it can operate the object by the low consumed electric current and it changed gain is securable.
[0009]
[Means for Solving the Problem] In order to attain the above-mentioned object, invention according to claim 1 The 1st transistor which inputs a RF signal into a gate electrode, and the 2nd transistor which outputs the RF signal concerned from a drain electrode, An inductor element or a resistance element for connecting between a drain electrode of the 1st transistor of the above, and a source electrode of the 2nd transistor of the above, and enlarging the above-mentioned inter-electrode RF-isolation, A capacitative element which makes low a RF-impedance in a source electrode of the 2nd transistor of the above, An implication and the 1st and 2nd transistors of the above are the RF gain adjustable amplifying circuits considered as a configuration which shares current from a power supply to a serial. As a variable resistive element to which gain acquired with the 1st and 2nd transistors of the above, without changing a RF-output impedance of the 2nd transistor of the above is changed It is characterized by connecting to a serial a resistance element arranged to the 3rd transistor and the drain source inter-electrode of this 3rd transistor to the above-mentioned inductor element or a resistance element between the above 1st and the 2nd transistor. Invention according to claim 2 is connected between a drain electrode of the 1st transistor of the above, and a gate electrode of the 2nd transistor of the above. Gain adjustable control voltage impressed to a gate electrode of the 3rd transistor of the above which carries out adjustable [of the gain which prepares the 4th transistor which operates as a signal attenuator, and is acquired from the 1st and 2nd transistors of the above] It connects also with a gate electrode of the 4th transistor of the above. Between a drain electrode of the 4th transistor of the above, and the above-mentioned power supplies, Between a drain electrode of this 4th transistor, a source electrode of between touch-down potentials and the 4th transistor of the above, the above-mentioned power supply, or touch-down potential It is characterized by connecting a bias resistance element for amending the linearity of dip of comprehensive gain variable characteristics over gain adjustable control voltage of a signal damping property with the 4th transistor of the above which considered gain variable characteristics with the 3rd transistor of the above.
[0010] Invention according to claim 3 is characterized by constituting the above-mentioned bias resistance element arranged to a source electrode side of the 4th transistor of the above so that bias resistance of a gate electrode of the 2nd transistor of the above may also serve. Invention according to claim 4 connects a resistance element and a capacitative element to a serial each drain gate inter-electrode of the 1st transistor of the above, and the 2nd transistor. It is characterized by connecting an inductor element for constituting the 1st transistor of the above, and the 2nd transistor as wideband amplifier, seeing from this input terminal between the above-mentioned input terminal and a gate electrode of the 1st transistor of the above, and amending an input reflection property in specific frequency. Invention according to claim 5 is characterized by forming a gain adjustable amplifying circuit of the above-mentioned configuration as an integrated circuit.
[0011] Since according to the configuration of above-mentioned claim 1 the 1st and 2nd transistors will share power supply current to a serial like before rather than will be parallel, it

can be made to operate by low current. Moreover, since gain adjustable control is performed by the 3rd transistor and resistance element with a variable-resistance function and the source of the 2nd transistor is grounded in RF by capacitative element, deterioration of output reflexibility at the time of gain adjustable can be controlled good.
[0012] According to the configuration of above-mentioned claim 2, by operating the 4th transistor as a signal attenuator, gain adjustable width of face can be enlarged and the linearity of dip of comprehensive gain variable characteristics can be improved by choosing a value of a bias resistance element suitably. Since a bias resistance element by the side of a source electrode of the 4th transistor and a bias resistance element of a gate electrode of the 2nd transistor were shared, while the number of resistance elements becomes fewer according to the configuration of above-mentioned claim 3, it becomes unnecessary [a capacitative element of DC cut arranged among these transistors].
[0013] According to the configuration of above-mentioned claim 4, although it becomes a broadband gain adjustable amplifying circuit, since amendment of the input reflection property of specific frequency in this case is performed, in actuation which carries out gain adjustable, deterioration of an input reflection property is small maintainable in a broadband. According to the configuration of above-mentioned claim 5, the number of terminals can be reduced compared with a case where it does not integrated-circuit-ize.
[0014]
[Embodiment of the Invention] The configuration of the RF gain adjustable amplifying circuit concerning the 1st example of an operation gestalt is shown in drawing 1 , and it sets to drawing 1 . Although 2nd FET2 for improving 1st FET1 of dual structure and an output reflection property between the input terminal T1 of a RF signal and the output terminal T2 of the RF signal concerned and 3rd FET3 which bears a variable-resistance function (it mentions later for details) are arranged These FET 1-3 is arranged to a power supply at a serial. that is, it is illustrated between power supply terminal T four and a gland (GND) -- as -- drain electrode [of 2nd FET2] (it considers as drain below) -> -- drain [of the source electrode (it considers as the source below) ->3rd FET3] -> -- drain [of the source ->1st FET1] (DC cut is carried out by capacity 38) -> -- it connects in order of the source. By this, these FET 1-3 will share power supply current directly.
[0015] The 1st above FET 1 is the amplifier of an auto-bias method, the auto-bias of the source is carried out by resistance 10, and bias of the gate electrode (it considers as the gate below) is carried out to touch-down potential by resistance 9. The RF-impedance is lowered by capacity 11 and, as for the source of this 1st FET1, affects it in [the impedance between this source and touch-down potential] RF with it. And the 2nd gate of this FET1 is short-circuited to that source. Moreover, resistance 22 and capacity 23 are connected to a serial the drain gate inter-electrode of this 1st FET1, by this, negative feedback is constituted and FET1 concerned is operated as wideband amplifier.
[0016] It is the amplifier of a fixed-bias method, and bias of that gate is carried out to the voltage which divided supply voltage by resistance 24 and resistance 25, and also in this 2nd FET2, with the resistance 26 and capacity 27 which have been arranged to the serial that drain gate inter-electrode, the 2nd above FET 2 constitutes negative feedback, and operates it as wideband amplifier.
[0017] And although the inductor 18 (resistance may be arranged instead of this inductor) for making the RF-isolation between these both high between the source of this 2nd FET2 and the drain of the 1st above FET 1 is arranged In order to achieve the variable-resistance function at the time of gain adjustable between this inductor 18 and the source of 2nd FET2, the 3rd above FET 3 and resistance 29 (this is arranged to the drain source inter-electrode of 3rd FET3) are connected to juxtaposition. Gain adjustable control voltage terminal T3 is arranged through resistance 30 at the gate of this 3rd FET3. According to this variable-resistance function, the gain of the 1st above FET 1 can be changed by using the voltage drop generated here and changing the voltage concerning the drain of the 1st above FET 1.
[0018] Moreover, the source electrode of this 2nd FET2 is grounded to GND in RF by capacity 32, and since the property of amplifier does not change greatly if the direct current

voltage in this source electrode does not change at the time of gain adjustable, deterioration of the output reflection property of 2nd FET2 concerned at the time of gain adjustable becomes small.

[0019] Furthermore, 4th FET4 is connected between 1st above-mentioned FET1 and 2nd FET2, and this is operated as a RF attenuator in the interstage of the wideband amplifier which consists of FET 1 and 2. That is, the voltage which pressured supply voltage partially by resistance 33 and resistance 34 is set up as bias voltage of the drain of this 4th FET4, and pull-up of the bias voltage of the source of this 4th FET4 is carried out to supply voltage by resistance 35. And the gate of this 4th FET4 is connected to control voltage terminal T3 mentioned above through resistance 36.

[0020] Between the drain sources of FET4 concerned will be in switch-on, and 4th FET4 as this RF attenuator spends for the bias which pressured supply voltage partially by the above-mentioned resistance 33, the juxtaposition combined resistance of resistance 35, and the above-mentioned resistance 34 to the drain and the source of the 4th above FET 4 at this time, when a damping property is min. And by impressing bias which is different in the 4th drain and source of FET4 with these resistance, the dip of a damping property can be adjusted and the linearity of the dip of the comprehensive gain variable characteristics over the gain adjustable control voltage of the signal damping property by the 4th above FET 4 in a form including the gain variable characteristics which 3rd FET3 has can be improved.

[0021] Moreover, between the gate of the 2nd above FET 2, and the source of 4th FET4, the capacity 37 for carrying out DC (direct current) cut is arranged, and the capacity 38 for DC cut is formed also between the drain of this 4th FET4, and the drain of 1st FET1 so that it may be illustrated. Furthermore, although the inductor 40 for improving an input reflection property is connected through capacity 39 between the above-mentioned input terminal T1 and the gate of 1st FET1 and being mentioned later for details, in the amplifier which carries out the gain adjustable, improvement in the input reflection property of specific frequency can be aimed at by this inductor 40 in a broadband.

[0022] Since according to such 1st-example configuration 1st FET1 - 3rd FET3 will share power supply current to a serial as mentioned above, it can be made to operate by low current. Moreover, between the source of 2nd FET2, and an inductor 18, since 3rd FET3 and resistance 29 with a variable-resistance function have been arranged, control voltage cannot be given like before to the 2nd gate of 1st FET1, but gain adjustable control can be performed by the variable-resistance function between 1st FET1 and 2nd FET2.

[0023] That is, the gain adjustable control voltage Vc impressed to above-mentioned terminal T3 is given to the gate of the 3rd above FET 3 through resistance 30, the resistance of a variable-resistance portion becomes small and the gain of the 1st above FET 1 becomes large, so that this control voltage Vc is higher than the source voltage Vs of the 2nd above FET 2. On the other hand, the resistance of a variable-resistance portion becomes large and the gain of the 1st above FET 1 becomes small, so that the gain adjustable control voltage Vc concerned is lower than the source voltage Vs of the 2nd above FET 2. And in such gain adjustable control, since the source of 2nd above-mentioned FET2 is grounded in RF with capacity 32, the voltage of this source electrode does not change but deterioration of an output reflection property becomes small.

[0024] Change of the source voltage of the 2nd above FET 2 at the time of changing gain, the drain voltage of 1st FET1, and source voltage is shown in drawing 4 . This graph is the property of each voltage when setting supply voltage (VDD) to 3V, and changing gain adjustable control voltage (Vc) to 0-3V as the 1st thru/or 3rd FET 1-3, using the field-effect transistor of GaAs(gallium arsenide) MES (Metal Semiconductor) whose pinch off voltage is -1V. As shown in this drawing 4 , even if the source voltage of 2nd FET2 changes gain, it will hardly change, but there will be no change in the direct-current bias of each electrode of 2nd FET2, and it is understood that deterioration of an output reflection property is small.

[0025] In the RF gain adjustable circuit of the 1st example of the above-mentioned operation gestalt, the property of the drain voltage of 4th FET4 when changing gain adjustable control voltage (Vc) into the 1st thru/or 4th FET 1-4 to 0-3V using GaAsMESFET whose pinch off

voltage is −1V like the above, having used supply voltage as 3V, and source voltage is shown in drawing 5 .

[0026] When control voltage becomes lower than 1V, the 4th drain voltage concerned and source voltage of FET4 of the 1st example are set up so that different voltage may be impressed, and can maintain the dip of comprehensive gain variable characteristics in a straight line mostly by this, so that it may be illustrated. About the linearity of this dip, it mentions later as compared with other examples of an operation gestalt.

[0027] The 2nd-example configuration of an operation gestalt is shown in drawing 2 . In this RF gain adjustable amplifying circuit as well as the 1st above-mentioned example between an input terminal T1 and an output terminal T2 The 1st FET1, 2nd FET2, and 3rd FET3 look at touch-down potential from power supply terminal T four. It connects so that power supply current may be shared to a serial, and between this 1st FET1 and 2nd FET2, 4th FET4 is connected and this is operated as a RF attenuator in the interstage of the wideband amplifier (it consists of 1st and 2nd FET 1 and 2).

[0028] And in this 2nd example, the bias voltage of the drain of the 4th above FET 4 carries out pull-up to supply voltage by the resistance 33 of drawing, the bias voltage of the source of the 4th above FET 4 is set up on the voltage which pressured supply voltage partially by resistance 24 and resistance 25 of drawing, and the resistance 24 and 25 it is [resistance] the bias resistance of the gate of the 2nd above FET is used also as bias resistance of 4th FET4.

[0029] That is, since this the 4th drain and source of FET4 show the same property, the resistance 33 and 34 by the side of the drain of 4th FET4 of the 1st example is arranged to a source side, and, on the other hand, they can arrange the resistance 35 by the side of the source to a drain side. Then, the 2nd example can share the bias resistance of the gate of 2nd FET2, and the bias resistance of the source of 4th FET4 by substituting resistance 24 and 25 for the 1st-example resistance 33 and 34, and substituting resistance 33 for resistance 35. According to this 2nd example, while being able to reduce the number of resistance elements, the capacity 37 which carries out the duty of DC cut also becomes unnecessary, and has the advantage that the cutback of components mark is achieved.

[0030] The 3rd-example configuration of an operation gestalt is shown, and also when it is this 3rd example, the connection configuration attached to 1st FET1 thru/or 4th FET4, and it which were mentioned above becomes being the same as that of the 1st example at drawing 3 . And in this 3rd example, the voltage further set as the drain and the source of the 4th above FET through resistance 44 and resistance 45 to the voltage which pressured supply voltage partially by resistance 42 and resistance 43 is given.

[0031] There is an advantage that deterioration of an output reflection property is small maintainable, by being able to connect 1st FET1 to 3rd FET3 to series on one power supply line, being ablė to make it operate by low current, and forming the capacity 32 for 3rd FET3 and the variable-resistance function of resistance 29, and RF-touch-down also by such 3rd example.

[0032] The gain variable characteristics (a continuous line and the 2nd example are expressed with a dotted line, and the 3rd example is expressed with the chain line for the 1st example) of the frequency in each circuit of the 1st above-mentioned example, the 2nd example, and the 3rd example are shown in drawing 6 . This drawing 6 is a property about the frequency of 1.5GHz, and in the range of 40dB or more, the gain adjustable is possible for it in all examples so that I may be understood from this drawing. And as for the circuit of the 1st example and the 2nd example, the linearity of the dip of gain variable characteristics is improved rather than the circuit of the 3rd above-mentioned example.

[0033] The 1st example and the 2nd example namely, by adjusting the value of the bias resistance 24, 25, 33-35 of each electrode of 4th FET4 As opposed to the linearity of the comprehensive gain variable-characteristics dip which considered the gain variable characteristics given by 3rd FET3 being improved in the case of this 3rd example Since the 4th drain and source of FET4 serve as the always same voltage, it is because the linearity of the dip of the comprehensive gain variable characteristics over the gain adjustable control

voltage in the condition that the signal damping property of the 4th above FET 4 was given is not compensated.
[0034] Furthermore, in the RF gain adjustable circuit of the 1st example thru/or the 3rd example of the above-mentioned operation gestalt, as mentioned above, the inductor 40 is formed between an input terminal T1 and 1st FET1, and when operating what was constituted as a gain adjustable amplifying circuit of a broadband by this inductor 40 on narrow-band frequency, the input reflection property in the specific frequency at the time of gain adjustable can be improved.
[0035] The input VSWR (voltage standing wave ratio) property (continuous line) when performing gain adjustable control with gain adjustable control voltage about the specific frequency of 850MHz in the circuit of the 1st above-mentioned example and an output VSWR property (dotted line), and the input VSWR property (chain line) when removing the above-mentioned inductor 40 from this 1st example circuit are shown in drawing 7 . According to this drawing 7 , it turns out that it is good compared with a property in case the property of the 1st example of a continuous line does not contain the inductor 40 of the chain line.
[0036] Moreover, as for the circuit of each above-mentioned example, integrated-circuit-izing is desirable, and according to this, it can lessen the number of terminals. That is, six terminals must be prepared, if the power supply terminal to an inductor 18 is required, considering the case where it does not integrated-circuit-ize by conventional drawing 8 and this and a GND terminal are added. On the other hand, in this invention, as shown in each drawing, it becomes five added the GND terminal to input/output terminals T1 and T2, gain control voltage terminal T3, and power supply terminal T four, and the number of terminals will become fewer.

[0037]
[Effect of the Invention] Since it considered as the configuration which looks at touch-down potential for the 1st transistor of the input side of a RF gain adjustable amplifying circuit, and the 2nd transistor of an output side from a power supply terminal, and shares this power supply current to a serial according to invention of claim 1 as explained above, actuation by low current is attained and it can contribute to power-saving. Moreover, while arranging the 3rd transistor and resistance element for gain adjustable between the 1st and the 2nd transistor of serial arrangement Since the capacitative element for RF-touch-down was connected between the source and touch-down potential of the 2nd transistor The gain of the 1st transistor of the above is changed in the condition of not changing the RF-output impedance of the 2nd transistor of the FET2 above, and it becomes possible to control deterioration of the output reflexibility at the time of gain adjustable.
[0038] Since the bias resistance element was prepared while according to invention of claim 2 and claim 3 arranging the 4th transistor between the signal lines of the above 1st and the 2nd transistor and adding the function of a RF signal attenuator, in order to enlarge gain adjustable width of face of the amplifying circuit concerned, the RF gain adjustable amplifier with which the 3rd transistor and 4th transistor interlock with one gain adjustable control voltage is constituted. Moreover, it becomes possible by adjusting the signal damping property of the 4th transistor with bias voltage to improve the linearity of the dip of the comprehensive gain variable characteristics over the gain adjustable control voltage of a signal damping property with the 4th transistor of the above which considered the gain variable characteristics given with the 3rd transistor.
[0039] And according to invention of this claim 3, since the bias resistance by the side of the gate of the 2nd transistor and the bias resistance by the side of the source of the 4th transistor were shared, the capacitative element for bias resistance and DC cut becomes unnecessary, and there is an advantage that the mark of a circuit element can be reduced.
[0040] Since according to invention of claim 4 the inductor is arranged between the gate of this 1st transistor, and an input terminal and the input reflection property in the specific frequency in a predetermined band was made good by the case where added the negative feedback circuit to the above 1st and the 2nd transistor, and it considers as the gain adjustable amplifying circuit of a broadband, it becomes possible to improve deterioration of

the input reflection property at the time of gain adjustable.
[0041] According to invention of claim 5, there is an advantage that the amplifying circuit which was stabilized with few terminals and which operates is obtained, by using the amplifier of above-mentioned claim 1 thru/or claim 4 as an integrated circuit.

[Translation done.]

* NOTICES *

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DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is drawing showing the configuration of the RF gain adjustable amplifying circuit concerning the 1st example of the operation gestalt of this invention.
[Drawing 2] It is drawing showing the configuration of the RF gain adjustable amplifying circuit concerning the 2nd example of an operation gestalt.
[Drawing 3] It is drawing showing the configuration of the RF gain adjustable amplifying circuit concerning the 3rd example of an operation gestalt.
[Drawing 4] In the circuit of the 1st example, it is the graph which shows the property of the source electrode voltage of the 1st FET when changing gain adjustable control voltage and drain electrode voltage, and the source electrode voltage of the 2nd FET.
[Drawing 5] In the circuit of the 1st example, it is the graph which shows the property of the drain electrode voltage of the 4th FET when changing gain adjustable control voltage, and source electrode voltage.
[Drawing 6] In the circuit of the 1st example, the 2nd example, and the 3rd example, it is the graph which shows the gain property (a continuous line and the 2nd example are expressed with a dotted line, and the 3rd example is expressed with the chain line for the 1st example) when changing gain adjustable control voltage.
[Drawing 7] In the circuit of the 1st example, it is the graph which shows the input VSWR property (chain line) at the time of removing an inductor element from the input VSWR property (continuous line) when changing gain adjustable control voltage and an output VSWR property (dotted line), and the 1st example circuit.
[Drawing 8] It is drawing showing the configuration of the conventional RF gain adjustable amplifying circuit.
[Description of Notations]
T1 — An input terminal, T2 — An output terminal, T3 — Gain adjustable control voltage terminal, T four — A power supply terminal, 1 — The 1st FET, 2 — The 2nd FET, 3 — The 3rd FET, 4 — The 4th FET, 6 — Input matching circuit, 7 — An output matching circuit, 9, 10, 13, 16, 22, 24, 25, 26, 29, 30, 33–36, 42–45 — A resistance element, 11, 14, 20, 21, 23, 27, 32, 37–39 — A capacitative element, 18, 19, 40 — Inductor element.

[Translation done.]

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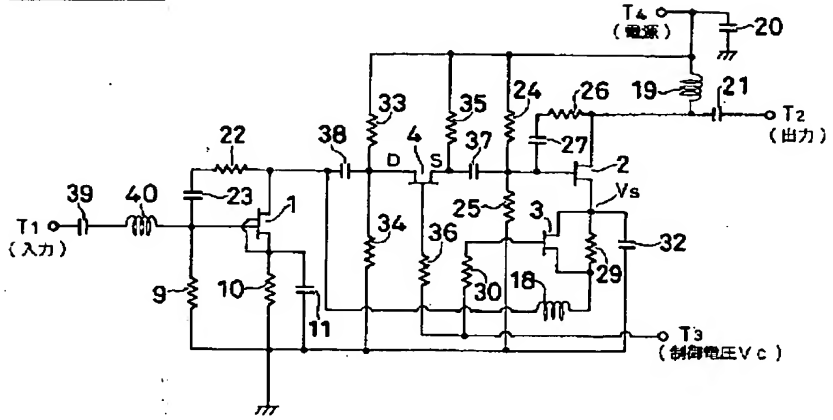
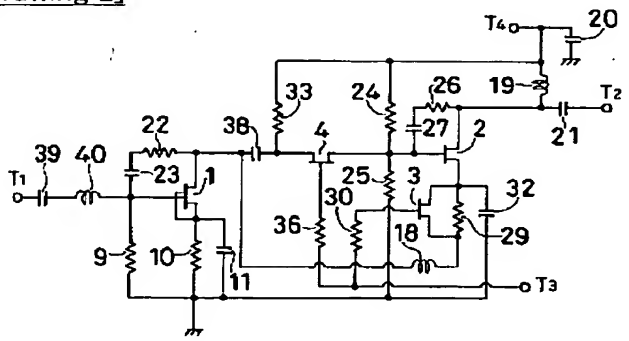
DRAWINGS

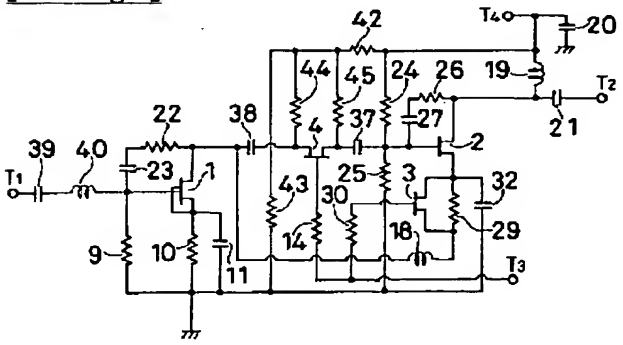
[Drawing 1]



[Drawing 2]



[Drawing 3]



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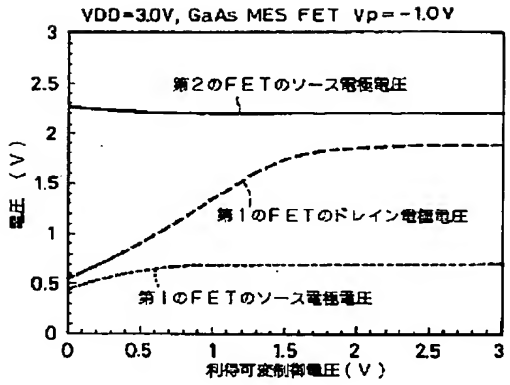

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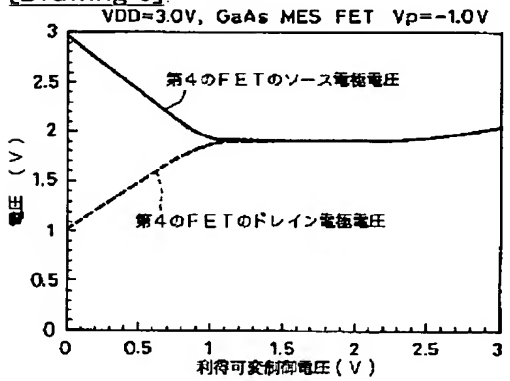

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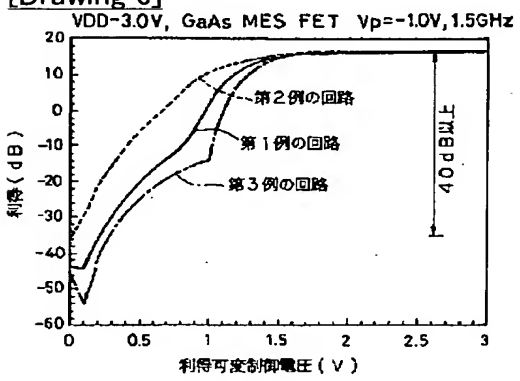
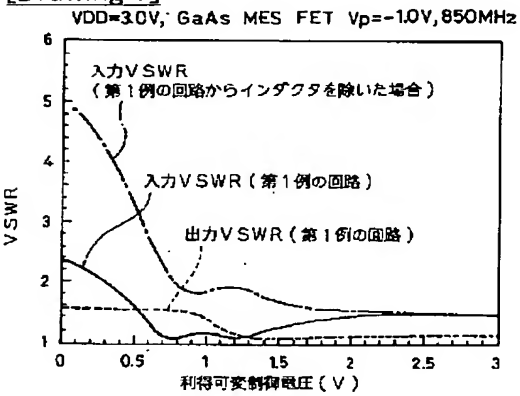
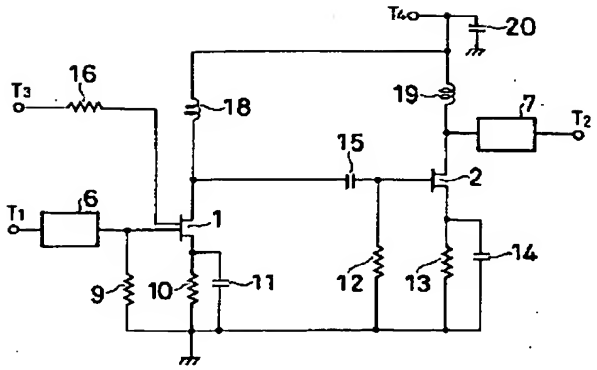


[Drawing 7]



[Drawing 8]



[Translation done.]